§ 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Claims:

Please substitute the following claim 1 for the pending claim 1:

1. (once amended) In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:

loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of the aligned vector to be generated;

loading a second vector from the memory unit into a second register;

determining a starting byte in the first register wherein the starting byte specifies the first byte of the aligned vector;

extracting the aligned vector from the first register and the second register beginning from the first bit in the starting byte of the first register continuing through bits in the second register; and

replicating the aligned vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.